AMENDMENTS TO THE CLAIMS

Cancel claims 6 and 13-24 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A charge pump comprising:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node, ~~and~~ a second input coupled to the second common drain node and an output directly coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input directly coupled to the first common drain node and a second input coupled to the reference circuit.

2. (Original) The charge pump of claim 1, further comprising a capacitor coupled to the first common drain node.

3. (Original) The charge pump of claim 1, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and

a fourth current source coupled to a source terminal of the third NMOS transistor;

wherein the second input of the second operational amplifier is coupled to the third common drain node.

4. (Original) The charge pump of claim 1, wherein the first current source is a PMOS current source.

5. (Original) The charge pump of claim 1, wherein the second current source is an NMOS current source.

6. (Canceled)

7. (Currently amended) The charge pump of claim 1, wherein an output of the second operational amplifier is directly coupled to a gate terminal of the first current source.

8. (Currently amended) An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node and having a second input and an output both directly coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input directly coupled to the first common drain node, a second input coupled to the reference circuit, and an output coupled to a gate terminal of the first current source.

9. (Original) The apparatus of claim 8, wherein the charge pump further includes a capacitor coupled to the first common drain node.

10. (Original) The apparatus of claim 8, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and

a fourth current source coupled to a source terminal of the third NMOS transistor;

wherein the second input of the second operational amplifier is coupled to the third common drain node.

11. (Original) The apparatus of claim 8, wherein the first current source is a PMOS current source.

12. (Original) The apparatus of claim 8, wherein the second current source is an NMOS current source.

13-24. (Canceled)

25. (Currently amended) A charge pump comprising:

an output terminal;

a first element to control charging of the output terminal;

a second element to control discharging of the output terminal and including a common node with the first element;

a reference circuit; and

an operational amplifier including a first input directly coupled to the ~~common node~~ output terminal and a second input directly coupled to the reference circuit.

26. (Previously presented) The charge pump of claim 25, wherein the first element comprises a first transistive element and the second element comprises a second transistive element.

27. (Previously presented) The charge pump of claim 26, wherein the first element comprises a PMOS transistor and the second element comprises an NMOS transistor.

28. (Previously presented) The charge pump of claim 25, wherein the reference circuit includes:

a first transistive element;

a second transistive element coupled to the first transistive element;

a first current source coupled to the first transistive element; and

a second current source coupled to the second transistive element.

29. (Previously presented) The charge pump of claim 28, wherein the first transistive element comprises a PMOS transistor and the second transistive element comprises an NMOS transistor.

30. (Previously presented) The charge pump of claim 29, wherein:

the first and second transistive elements include a common drain node; and

the second input of the operational amplifier is coupled to the common drain node.

31. (Previously presented) The charge pump of claim 25, further comprising:

a second output terminal; and

a second operational amplifier including a first input coupled to the common node and including a second input coupled to the second output terminal.

32. (Currently amended) An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

an output terminal;

a first element to control charging of the output terminal;

a second element to control discharging of the output terminal and including a common node with the first element;

a reference circuit; and

an operational amplifier having a first input directly coupled to the ~~common node~~ output terminal and a second input coupled to the reference circuit.

33. (Previously presented) The apparatus of claim 32, wherein the first element comprises a first transistive element and the second element comprises a second transistive element.

34. (Previously presented) The apparatus of claim 33, wherein the first element comprises a PMOS transistor and the second element comprises an NMOS transistor.

35. (Previously presented) The apparatus of claim 32, wherein the reference circuit includes:

a first transistive element;

a second transistive element coupled to the first transistive element;

a first current source coupled to the first transistive element; and

a second current source coupled to the second transistive element.

36. (Previously presented) The apparatus of claim 35, wherein the first transistive element comprises a PMOS transistor and the second transistive element comprises an NMOS transistor.

37. (Previously presented) The apparatus of claim 36, wherein:

the first and second transistive elements include a common drain node; and

the second input of the operational amplifier is coupled to the common drain node.

38. (Currently amended) The apparatus of claim 32, wherein the charge pump further includes:

a second output terminal; and

a second operational amplifier ~~include~~ including a first input coupled to the common node and include a second input coupled to the second output terminal.